UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	000808	Total Pages	
First Named Inventor or Application Identifier			
Yoshihiro MIYAMOTO			
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APPLICATION ELEMENTS FOR:

SOLID-STATE IMAGING DEVICE

ADDRESS TO: Director of Patents and Trademarks
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Washington, D.C. 20231

1. [XX] Fee Transmittal Form (Incorporated within this form)
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2. [XX] Specification Total Pages [**38**]

3. [XX] Drawing(s) (35 USC 113) Total Sheets [**11**]

4. [XX] Oath or Declaration Total Pages [**5**]

a. [XX] Newly executed (original)

b. [ ] Copy from prior application (37 CFR 1.63(d)
(for continuation/divisional with Box 17 completed).

i. [ ] Deletion of Inventor(s)
Signed statement attached deleting inventor(s) named in prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. [ ] Incorporation by reference (useable if box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program (Appendix)

7. [ ] Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

a. [ ] Computer Readable Copy
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c. [ ] Statement Verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [XX] Assignment Papers (cover sheet and document(s))

9. [ ] 37 CFR 3.73(b) Statement (when there is an assignee) [XX] Power of Attorney

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10. [ ] English translation Document (if applicable)

11. [XX] Information Disclosure Statement **[3]** Copies of IDS Citations

12. [ ] Preliminary Amendment

13. [XX] Return Receipt Postcard (MPEP 503)

14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application Status still proper and desired.

15. [XX] Claim for Convention Priority **[1]** Certified copy(ies) of Priority Document(s)

a. Priority of _____ application no. _____ filed on _____ is claimed under 35 USC 119. The certified copies/copy have/has been filed in prior application Serial No. _____.
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[XX] A check in the amount of $ **730.00** is enclosed to cover the filing fee of $ 690.00 and the assignment recordation fee of $40.00.

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SOLID-STATE IMAGING DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a solid-state imaging device constituted by a semiconductor device, and more particularly to an XY address-type solid-state imaging device manufactured by a CMOS process. In addition, the present invention relates to a solid-state imaging device capable of eliminating the effects of fixed pattern noise and thermal noise.

2. Description of the Related Art

Solid-state imaging devices include XY address-type solid-state imaging devices in which an image sensor is formed by CMOS, and the so-called CCD solid-state imaging devices constituting a charge transfer-type image sensor. Because the XY address-type solid-state imaging device, which utilizes a CMOS image sensor, does not require a special manufacturing process, and is driven by a single power source with smaller power consumption, and furthermore, is capable of mounting various signal processing circuits on the same chip, it is seen as a promising replacement for CCD solid-state imaging devices.

This CMOS image sensor-equipped conventional XY

address-type solid-state imaging device will be explained by using Fig. 7. Fig. 7 shows an example circuit worth of one picture element (pixel) of a conventional XY address-type image sensor. The conventional CMOS image sensor shown in Fig. 7 has a constitution called an APS (Active Pixel Sensor), which mounts a source follower or other such buffer 404 to each pixel. The cathode side of a photodiode 400 is connected to the gate electrode of the buffer 404, and to an MOSFET reset switch 402. Further, buffer 404 is connected to a vertical selection line 408 via a horizontal selection switch 406.

The operation of this conventional XY address-type solid-state imaging device will be briefly explained. First, when reset switch 402 is turned ON at a prescribed timing by a reset signal RST, photodiode 400 is charged to a reset potential VRST. Next, the discharge of photodiode 400 commences in line with an incoming light, and the potential decreases from the reset potential VRST. After the passage of a prescribed time, when a horizontal selection signal RWn is input to the gate electrode of horizontal selection switch 406, and horizontal selection switch 406 transitions ON, a source voltage of buffer 404 is extracted as a signal voltage via vertical selection line 408.

However, a conventional APS of the above constitution has a charge storage capacitor and a source follower or other such amplifier, a fixed pattern noise (FPN) in

generated. This noise is DC output level fluctuation for the same signal according to VT (threshold voltage) variation of the source follower transistor. It results in picture quality deterioration. That is, the detection voltage varies between cells for the same quantity of light received, resulting from built-in variations in the threshold voltage VT of the source follower transistor 404.

To reduce this variation, in the conventional device, after sampling an integral level conforming to a quantity of received light as a source signal voltage V1 of buffer 404, photodiode 400 is reset to the reset potential VRST, and this reset voltage is sampled. Then, fixed pattern noise is reduced by determining, using a correlated double sampling (CDS) circuit, the voltage difference between a source signal voltage V2 corresponding to reset voltage VRST and the above-mentioned source signal voltage V1. In other words, by sampling a reset voltage after storing a quantity-of-light signal, and determining, via a correlated double sampling circuit (CDS circuit), the difference with the signal voltage at the time of storing the quantity-of-light signal, the effects of threshold voltage VT variations are removed, and the fixed pattern noise (FPN) is reduced.

However, with this method, there remains the problem that the reset noise (kTC noise) before storing a quantity-of-light signal and the reset noise after reading

the signal are added so as to increase the random noise level, and the S/N ratio deteriorates compared to that of a CCD solid-state imaging device.

kTC noise (where k is Boltzmann's constant, T is absolute temperature, and C is the capacitor of photodiode 400) is a kind of thermal noise. When reset switch 402 is made conductive by a reset signal RST, and photodiode 400 charges to a reset voltage VRST, the cathode terminal voltage of this parasitic capacitance is subject to the fluctuations of the thermal noise $4kTR\Delta f$ (where R is the resistance of reset switch 402, and Δf is the frequency range at charge time) from the reset voltage VRST. As a result thereof, the cathode terminal voltage resulting from a reset operation is not necessarily becoming a constant reset voltage VRST.

The above-mentioned conventional example uses the difference between a quantity-of-light signal level whose voltage drops from an initial reset level conforming to a quantity of received light, and a reset level of immediately thereafter. However, since this kTC noise has random fluctuations with time as hereinabove, the kTC noise that is superimposed on the initial reset level differs from the kTC noise that is superimposed on the second reset level, making it impossible to curb kTC noise even by using the difference between these two levels to curb fixed pattern noise (variations in threshold voltage VT).

Next, an XY address-type solid-state imaging device disclosed in Japanese Patent Application Laid-open No. 8-205034 will be explained by using Fig. 8. In Fig. 8, a source follower-type buffer B1 is connected between a frame transfer gate FT and an MOS-type switch SY1. Further, an MOSFET-constituted reset switch SR1 is connected to a second capacitor C2 for removing a charge that is stored in the second capacitor C2. The drain electrode of a buffer B1 is connected to a power source VDD, and the source electrode of the buffer B1 is connected to a horizontal selection switch SY1. Further, the gate electrode of buffer B1 is connected to second capacitor C2. Reset potential VR is applied to the drain electrode of reset switch SR1. The source electrode of reset switch SR1 is connected to the second capacitor C2, and the gate electrode of reset switch SR1 is connected to reset control signal line L2.

When a charge is transferred to the second capacitor C2 by making frame transfer gate FT conductive after a charge has been stored in a first capacitor C1, the gate potential of the buffer B1 steadily increases. When horizontal selection switch SY1 transitions ON after the passage of a prescribed time, the source voltage of buffer B1 is output via a vertical selection line, and a quantity of charge Q stored in the second capacitor C2 can be detected. By making reset switch SR1 conductive one time prior to making the frame transfer gate FT conductive,

all of the charge stored in the second capacitor C2 can be removed, making it possible to curb the deterioration of picture quality resulting from a residual image charge.

However, for the conventional example of Fig. 8, firstly, the problem is that because there is a buffer B1, which is a source follower, it is not possible to remove the effects of threshold voltage variations (fixed pattern noise) in the transistor B1, and the detection level between cells varies. Furthermore, in Japanese Patent Application Laid-open No. 8-205034, there is no disclosure at all that offers suggestions concerning curbing this fixed pattern noise. And it is also not possible to remove kTC noise, which is thermal noise generated at reset, because after the second capacitor C2 is charged to reset voltage VR, a charge that accords with a quantity of light is transferred via gate FT from the first capacitor C1, a voltage that accords with the quantity of light is lowered from reset voltage VR, and only this voltage is transferred to a charge readout portion.

Further, as for the device constitution of the pixel shown in Fig. 8, the problem is that there is at the least 1 more transistor than the device constitution of the pixel shown in Fig. 7 (2 if reset switch 402 shown in Fig. 7 is added), constitution of the pixel portion is complex, and the numerical aperture of the light reception portion (fill factor) decreases.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a solid-state imaging device, which reduces fixed pattern noise (FPN) and thermal noise.

Furthermore, another object of the present invention is to provide a solid-state imaging device, which has a wide numerical aperture with a simple pixel constitution, and which reduces the above-mentioned noise.

To achieve the above-mentioned objects, a first aspect of the present invention is a solid-state imaging device comprising: a plurality of pixels including a light-sensitive portion for photoelectrically converting incident light, a transfer gate for transferring a stored charge to the light-sensitive portion, a resettable detection capacitor for storing the charge transferred from the transfer gate, and a selection switch for outputting a charge of the detection capacitor according to a selection signal; a charge amplifier for converting the detection capacitor charge, which is output from the pixels, to a voltage; and a correlated double sampling circuit for obtaining a voltage difference between a reset level and a detected level converted by the charge amplifier.

In the above-mentioned solid-state imaging device of the present invention, it is desirable that the charge amplifier be a capacitive feedback-type impedance

conversion circuit. Further, the charge amplifier is characterized in that, in accordance with the detection capacitor being connected to the selection line by the selection switch transitioning to ON, the reset level of the detection capacitor is converted to a reset voltage, and next, the charge, which is transferred to the detection capacitor from the light-sensitive portion by the transfer gate transitioning to ON, is converted to a detected voltage. Furthermore, it is desirable for the charge amplifier to be connected to the correlated double sampling circuit via a sample holding circuit.

To achieve the above-mentioned objects, a second aspect of the present invention is a solid-state imaging device comprising: a plurality of pixels, having a light-sensitive portion for photoelectrically converting incident light and storing a charge, a reset gate, connected to the light-sensitive portion, for depleting the light-sensitive portion by becoming conductive in response to a reset signal, and a transfer gate, connected to the light-sensitive portion, for outputting a charge stored in the light-sensitive portion by becoming conductive in response to a selection signal; a charge amplifier, connected to the pixels, for converting the outputted charge to a voltage ; and a correlated double sampling circuit for sampling and holding the output voltage of the charge amplifier, and a differential voltage between a reset level, which the charge amplifier

outputs when being reset, and a detection level, which the charge amplifier outputs in accordance with a charge outputted from the pixels, is output from the correlated double sampling circuit.

According to the above-mentioned second aspect, it is possible to reduce the effects of thermal noise by making use of a differential voltage between a reset level on which a thermal noise is superimposed, and a detection level added thereto. Further, because a light-sensitive portion is depleted by the conduction of a reset gate, thermal noise is not superimposed on the potential (or voltage) level at reset. Furthermore, since there is no source follower or other such circuit in a pixel, fixed pattern noise is not generated.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram showing a circuit example of an XY address-type image sensor 1 in a solid-state imaging device according to a first embodiment of the present invention;

Fig. 2 is a diagram showing a circuit example of a charge amplifier in a solid-state imaging device according to the first embodiment;

Fig. 3 is a diagram showing a circuit example of a sample holding circuit and a correlated double sampling circuit in a solid-state imaging device according to the

first embodiment;

Fig. 4 is a diagram showing the cross-sectional structure of a pixel and potential schematics of an XY address-type image sensor according to the first embodiment;

Fig. 5 is a timing chart showing the operation of an XY address-type image sensor according to the first embodiment;

Fig. 6 is a diagram showing the results of simulation with a simplified circuit changes in output OUTm output from a charge amplifier of an XY address-type image sensor according to the first embodiment;

Fig. 7 is a diagram showing a conventional XY address-type solid-state imaging device, which uses a CMOS image sensor;

Fig. 8 is a diagram showing another example of a conventional XY address-type solid-state imaging device, which uses a CMOS image sensor;

Fig. 9 is a diagram showing a circuit example of an XY address-type image sensor in a solid-state imaging device according to a second embodiment;

Fig. 10 is the cross-sectional structure and energy level schematics of a solid-state imaging device in the second embodiment;

Fig. 11 is a timing chart showing the driving of a cell;

Fig. 12 is a diagram showing a variation of the second

embodiment; and

Fig. 13 is a diagram showing simulation results of the second embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be explained hereinbelow by referring to the figures. However, the technical scope of the present invention is not limited to such embodiments.

A solid-state imaging device according to a first embodiment of the present invention will be explained by using Fig. 1 through Fig. 6. First, a simplified constitution of a solid-state imaging device according to the embodiment will be explained using Fig. 1.

Fig. 1 shows a circuit example of an XY address-type image sensor 1 corresponding to 2 x 2 pixels in a solid-state imaging device of the embodiment. MOSFET transfer gates (TG) 10, 12, 14, 16 are connected, respectively, to the cathode sides of photodiodes 2, 4, 6, 8 of the light-sensitive portions of each pixel. Furthermore, photodiode 2 in the light-sensitive portion can be constituted from a photogate. Source junction capacitors of the floating diffusion (FD) region of between transfer gates 10, 12, 14, 16 and MOSFET horizontal selection switches 26, 28, 30, 32 are used as detection capacitors 18, 20, 22, 24. The gate electrodes of

transfer gates 10, 12 are connected to transfer gate control line 62, and the gate electrodes of transfer gates 14, 16 are connected to transfer gate control line 70. The gate electrodes of horizontal selection switches 26, 28 are connected to horizontal connection line 64. The gate electrodes of horizontal selection switches 30, 32 are connected to horizontal connection line 72.

Further, MOSFET reset switches 34, 36, 38, 40 for charging detection capacitors 18, 20, 22, 24 to a reset level are connected respectively to the detection capacitors. The drain electrodes of reset switches 34, 36 are connected to reset voltage supply line 58 to which reset voltage VRS is supplied. The source electrodes of reset switches 34, 36 are connected to detection capacitors 18, 20 respectively, and the gate electrodes are connected to reset control signal line 60. The drain electrodes of reset switches 38, 40 are connected to a reset voltage supply line 66 to which reset voltage VRS is supplied. The source electrodes of reset switches 38, 40 are connected to detection capacitors 22, 24 respectively, and the gate electrodes are connected to reset control signal line 68.

Horizontal selection switches 26, 30 are connected to vertical selection line 54, and horizontal selection switches 28, 32 are connected to vertical selection line 56. Charge amplifiers (capacitive feedback-type impedance conversion circuits: CTIA) 41, 43 are connected

to vertical selection line 54, 56, respectively. As shown in Fig. 2, for example, charge amplifier 41, which is connected to vertical selection line 54, has a CMOS inverter 42, and feedback capacitor 46, in addition to an MOSFET line reset switch 50 for short circuiting feedback capacitor 46.

In Fig. 2, the block indicated by a broken line in the figure shows the pixel of the upper left of Fig. 1 as an example of the plurality of pixels connected to vertical selection line 54. When detection capacitor 18 is connected to vertical selection line 54 via horizontal selection switch 26, a voltage, which accords with a quantity of charge that is stored in detection capacitor 18, is output as output OUTm by charge amplifier 41, which is connected to vertical selection line 54. Furthermore, capacitors CLN, CLD in the figure indicate the parasitic capacitance of vertical selection line 54 (CLN), and the output terminal capacitance of charge amplifier 41 (CLD). Further, taking the fill factor into consideration, charge amplifier 42 can, of course, utilize a CMOS operational amplifier in place of a CMOS inverter.

Furthermore, output terminal OUTm is connected to the correlated double sampling circuit shown in Fig. 3, and the differential voltage between a reset level and a detected signal level, which accords with a quantity of light, is detected.

Returning to Fig. 1, similarly, charge amplifier 43,

which is connected to vertical selection line 56, has, for example, a CMOS inverter 44, a feedback capacitor 48, and a line reset switch 52 for short circuiting feedback capacitor 48. The gate electrodes of line reset switches 50, 52 are connected to line reset signal line 74, which resets vertical selection lines 54, 56.

As explained hereinabove, in the constitution of an XY address-type image sensor 1 according to the embodiment, a so-called active element (amplifier or the like) does not exist inside each of the pixels, which are provided in a 2-dimensional (of course, 1-dimensional is also fine) layout. More specifically, a source follower-type amplifier, like buffer 404 shown in Fig. 7, or buffer B1 shown in Fig. 8, is not connected between the transfer gates 10, 12, 14, 16 and the horizontal selection switches 26, 28, 30, 32. Taking the pixel in the upper left of Fig. 1 as an example, the main components inside 1 pixel comprise only a light-sensitive portion photodiode 2, a resettable detection capacitor 18, a transfer gate 10 for controlling the transfer of a charge from the light-sensitive portion, a reset switch 34, and a horizontal selection switch 26, which connects the detection capacitor 18 to a vertical selection line 54. A change in the charge of a detection capacitor 18 of a pixel selected from among the plurality of pixels connected to the vertical selection line 54 is detected by the charge amplifier 41, which is connected to vertical selection

line 54. In this manner, 1 pixel has a photodiode 2, and 3 transistors (10, 26, 34), making the number of elements the same as the conventional APS shown in Fig. 7, and 1 (or 2) less than the conventional APS shown in Fig. 8. Further, with the constitution of the embodiment, because it is possible to achieve a simple element composition, which uses 3 small, current-driving-capable transistors, there is no need for a source follower driving transistor for driving vertical selection line 54, thus enabling the fill factor to be improved.

Next, specific examples of a sample holding circuit, and a correlated double sampling (CDS) circuit will be briefly explained by using Fig. 3. The circuitry of Fig. 3 is provided to vertical selection lines 54, 56, respectively, of Fig. 1. A sample holding capacitor 78 for holding an inputted output OUTm is connected to an MOSFET sample holding switch 76 for controlling the input of output signal OUTm from charge amplifier 41. Further, a source follower-type buffer 82 is connected to the connection N3 of switch 76 and sample holding capacitor 78. The output N1 of buffer 82 is connected to a CDS capacitor 86 of the correlated double sampling circuit, and the other terminal N2 of CDS capacitor 86 is connected to source follower-type buffer 88. Furthermore, source follower-type buffer 88 is utilized in this sample holding circuit/correlated double sampling circuit, but, of course, these circuits can also be constituted by a voltage

follower.

A clamping switch 84 is connected to the connection N2 between CDS capacitor 86 and source follower-type buffer 88. Buffer 88 is connected to a multiplexing switch 90, and multiplexing switch 90 is connected to a common bus interconnect 94. In this manner, the output of the correlated double sampling circuit is connected to common bus interconnect 94 by way of multiplexing switch 90, and is time multiplexed. Further, source follower-type buffer 88 of the correlated double sampling circuit, which is disposed on vertical selection lines 54, 56, respectively, is connected to a common load current source 92 by way of common bus interconnect 94.

Next, the operation of a solid-state imaging device according to the embodiment will be explained using mainly Fig. 4 and Fig. 5, while also referring to Fig. 1 through Fig. 3. Fig. 4 shows the cross-sectional structure and potential schematics of a pixel of an XY address-type image sensor 1 according to the embodiment. Fig. 5 is a timing chart showing the operation of XY address-type image sensor 1.

Fig. 4A shows the cross-sectional structure of the pixel in the upper left of Fig. 1, and an N- region constituting a PN junction photodiode 2 is formed inside a P well 100, which is formed inside an N-well region of a P-type substrate not shown in the figure. A dielectric layer 102 (comprising a gate dielectric layer and a field

dielectric layer) is formed on the P-well 100. From the perspective of the figure, transfer gate 10 and horizontal selection switch 26 are formed side by side, and reset switch 34 does not appear in this cross-section. The reset switch 34 is the opposite side of the N- region relative to the gate electrode of transfer gate 10, and the region between the gate electrode of the transfer gate 10 and the gate electrode of the horizontal selection switch 26 is an N+ layer floating diffusion (FD) region. The N+ region (BUS), which is formed on the opposite side of the FD region relative to horizontal selection switch 26, is connected to charge amplifier (CTIA) 41 by way of vertical selection line 54.

Furthermore, as shown in Fig. 4E, a photogate PHG can, of course, be used in place of photodiode 2 in the light-sensitive portion. The explanation hereinbelow can also be applied in the same manner to an XY address-type image sensor that uses the photogate shown in Fig. 4E. Further, because the photogate itself is known, an explanation of the constitution of Fig. 4E is omitted.

As shown in the timing chart of Fig. 5, a line reset signal LRST is output over line reset signal line 74 at timing t1 (refer to Fig. 4B), and at the same time, a reset signal RSTn (where n is a horizontal selection number) is output over reset control signal line 60. Charge amplifier 41 and vertical selection line 54 are reset by line reset signal LRST, and the FD region (detection

capacitor 18) is reset by reset signal RSTn to a reset voltage VRS from reset voltage supply line 58. At this time, the transfer gate 10 and horizontal selection switch 26 are both in the OFF state. Further, in a case in which charge amplifier 41 is constituted by the CMOS inverter 42 shown in Fig. 2, vertical selection line 54 and BUS are reset to a potential of near VDD/2, and voltage VDD/2 is output at charge amplifier output OUTm.

When light is irradiated, and a carrier is generated by photodiode 2, a charge is stored in the N- region. Because an energy barrier is formed by transfer gate 10 between photodiode 2 and the FD region, the charge in light charge storage stays in the N- region.

Next, at timing t2 (refer to Fig. 4C), when a horizontal selection signal RWn is input from horizontal selection line 64 to the gate of horizontal selection switch 26, and horizontal selection switch 26 transitions to ON, output OUTm = VR (reset voltage), which is equivalent to reset level VRS from charge amplifier 41, is output (refer to Fig. 5), and, in addition, the FD region and BUS region constitute the same potential of nearly VDD/2.

Subsequently, at timing t3 (refer to Fig. 4D), gate signal TGn is input to the gate of transfer gate 10 from transfer gate control line 62 with horizontal selection switch 26 in the ON state as-is. Transfer gate 10 transitions to the ON state in accordance with gate signal

TGn, the barrier under the gate disappears, and a charge stored in photodiode 2 is transferred to the FD region (charge detection capacitor 18). In this manner, the light-sensitive portion is constituted by the low-concentration reverse conductivity layer and the transfer gate, and at charge transfer time, the low-concentration reverse conductivity layer is controlled so as to be completely depleted. Furthermore, in a case in which the light-sensitive portion is constituted by a photogate and transfer gate as shown in Fig. 4E, the photogate is controlled so as to be completely depleted at charge transfer time.

A voltage change, which accords with this quantity of charge, is output as output OUTm = VS (signal voltage) from charge amplifier 41. The above operation is performed at a horizontal blanking period, and the reset voltage VR and the detected signal voltage VS are output from charge amplifier 41 in such sequence.

In this manner, in the embodiment, after the charge amplifier 41 and vertical selection line 54 are reset and at the same time the detection capacitor 18 is also reset at timing t1, the charge amplifier 41 is set to the detection mode. At timing t2, by setting the horizontal selection switch 26 to ON, and connecting the detection capacitor 18 to vertical selection line 54, the reset level of detection capacitor 18 is converted to reset voltage VR. And next, at timing t3, a charge is either injected

to or transferred from the light-sensitive portion 2, to the vertical selection line 54 and converted to the signal voltage VS.

The results of simulation via a simplified circuit the changes in output OUTm from charge amplifier 41 are shown in Fig. 6. The horizontal axis of Fig. 6 represents time (2μsec/div), and the vertical axis shows the output voltage of the output OUTm. Fig. 6 shows an example of a case in which a line reset signal LRST and a reset signal RST are output every 2μsec, a quantity of light increases, and a charge to be stored in the photodiode gradually increases. Letting VDD = 3V, OUTm = VDD/2 = 1.5V at line reset time, OUTm = VR is output by inputting a horizontal selection signal RWn, which is input immediately after line reset, the transfer gate 10 transitions to the ON state after approximately 1μsec from line reset, and OUTm = VS is output. In this way, in the embodiment, a reset voltage VR of immediately prior to signal storage is outputted from charge amplifier 41, and thereafter, signal voltage VS is output. Furthermore, as is clear from the timing chart of Fig. 5, because charge amplifier 41 according to the embodiment is constituted so as to be connected to a power source and activated only in the prescribed period of a detection mode, wherein a reset voltage VR and a signal voltage VS are detected and output, it is possible to strive for power savings.

Output OUTm from charge amplifier 41 is input to the

sample holding circuit and correlated double sampling circuit shown in Fig. 3. As shown in Fig. 5, at timing t2, a sample holding signal SH is input at the gate of sample holding switch 76 of the sample holding circuit in synchronization with the rising edge of reset voltage RSTn, transitioning switch 76 to the ON state. And at the same time, a clamping signal CLP is input at the gate of clamping switch 84 of the correlated double sampling circuit in synchronization with the falling edge of reset voltage RSTn, transitioning switch 84 to the ON state.

In this timing t2 state, OUTm = VR from the charge amplifier 41 is applied to the input terminal (IN) of the sample holding circuit. Reset voltage VR charges sample holding capacitor 78 of the sample holding circuit, and, in addition, also charges correlated double sampling capacitor 86 by way of source follower 82. Because in accordance with the ON state of clamping switch 84, the other terminal of correlated double sampling capacitor 86 is fixed at ground voltage, node N1 is charged by a voltage that is lower by the threshold voltage of source follower transistor 82 than the charging voltage (node N3 voltage) of sample holding capacitor 78.

Subsequently, at timing t3, at the point in time when the other terminal (node N2) of correlated double sampling capacitor 86 becomes floating by clamping switch 84 OFF, signal voltage VS is input to the input terminal of the sample holding circuit, and held by sample holding

capacitor 78. As a result thereof, a differential signal (VS-VR), which is equivalent to the difference between the reset voltage VR and the signal voltage VS, is generated at the output side (node N2) of correlated double sampling capacitor 86. This signal is held by correlated double sampling capacitor 86, and drives output source follower-type buffer 88. Output source follower-type buffer 88 is connected to a horizontal direction output line 94 by way of multiplexing switch 92, and only the differential signal (VS-VR) which offsets the reset noise is output.

The above operation is summarized as hereinbelow. This summary will be explained by referring to Fig.'s 2, 3, 4, 5. On the premise of reading out a charge that accords with a quantity of light received, charges stored in the photodiode of each cell are all read out at the stage of timing t3 (Fig. 4D).

During the horizontal blanking period of a cell, at reset timing t1, reset signal RSTn is applied, reset switch 34 conducts, and detection capacitor 18 is charged to reset voltage VRS. Specifically, as explained for the conventional example, the reset level of detection capacitor 18 constitutes the level at which kTC noise (thermal noise) is superimposed on reset voltage VRS. Further, at reset timing t1, because the feedback switch 50 of charge amplifier 41 transitions ON, the input and output of CMOS inverter 42 are both reset to an

intermediate of power source voltage VDD/2. As a result thereof, the level of readout line 54 (BUS region) constitutes VDD/2 as shown in Fig. 4B.

Following the above-mentioned reset timing t1, at reset level readout timing t2, the reset level of detection capacitor 18 is held in sample holding capacitor 78 and correlated double sampling capacitor 86. That is, when the horizontal selection switch 26 transitions to ON by the horizontal selection signal RWn, the potential of the capacitor CLN of vertical selection line 54, which is connected to the input of CMOS inverter 42, is maintained at VDD/2 by an image charging operation of the CMOS inverter 42 and feedback capacitor 46 thereof, and, in addition, a potential VR that accords with reset level VRS is generated at output OUTm. That is, as shown in Fig. 5, output OUTm is reduced to reset level VR by the image charging operation of charge amplifier 41. And then, the reset level of this output OUTm is held by sample holding capacitor 78, and at the same time, a charge corresponding thereto is also held in correlated double sampling capacitor 86. That is, the reset level is held in correlated double sampling capacitor 86, and the level, at which thermal noise (kTC noise) is superimposed on the reset level, is held in node N1.

Accordingly, a quantity of charge stored in the capacitor of photodiode 2, is read out at light integral value readout timing t3. Transfer gate 10 is set to ON

by gate signal TGn with horizontal selection switch 26 in the ON state as-is. As a result thereof, as shown in Fig. 4D, a charge stored in photodiode 2 flows into detection capacitor 18 and vertical selection line 54. At this time, the potential of the capacitor CLN of the vertical selection line 54, which is connected to the input of CMOS inverter 42, is maintained at VDD/2 by the image charging operation of CMOS inverter 42 and the feedback capacitor 46 thereof, and, in addition, as shown in Fig. 5, a detection level VS corresponding to a quantity of charge stored in photodiode 2 is generated at output OUTm. At this readout, the charge of photodiode 2 becomes void, constituting a completely depleted state.

By sampling and holding detection level VS read out at this output OUTm, node N1 of correlated double sampling capacitor 86 constitutes a level corresponding to detection level VS. As a result thereof, node N2, which is the counter electrode of capacitor 86, constitutes the differential potential (VS-VR) of reset level VR and detection level VS. However, this detection level VS is the level to which is added the thermal noise superimposed on the initial reset level VR. Therefore, thermal noise is eliminated by determining the differential potential thereof.

Moreover, the inside of a cell is not a constitution which is subject to the effects of the threshold voltage VT of a transistor such as a source follower circuit as

with a conventional example. Therefore, the differential potential (VS-VR) constitutes a signal, which does not comprise fixed pattern noise.

In the above-mentioned operation example, the storage period of a charge corresponding to a quantity of light received in photodiode 2 constitutes a period from after a readout until the next readout. Accordingly, in a case in which it is necessary to adjust this charge storage period to an arbitrary period, the transfer gate 10 can be set to ON by applying a gate signal TGn at the appropriate time, and a charge stored in photodiode 2 can be transferred to detection capacitor 18. In accordance therewith, in detection capacitor 18, as indicated by the dotted line in Fig. 4B, detection capacitor 18 is charged to a certain level. However, because detection capacitor 18 is reset to reset level VRS at reset timing t1, there is no effect on the readout level thereafter.

In this manner, according to the embodiment, because a charge is transferred, and a signal is detected after line reset and detection capacitor reset, reset noise (kTC noise) is offset by the correlated double sampling thereafter, and in principle, it is possible to achieve the same picture quality as a CCD-type solid-state imaging device with a CMOS-based circuit constitution without generating either fixed pattern noise or kTC noise.

The present invention is not limited to the above embodiment, and various variations are possible.

For example, in the above embodiment, an example in which a CMOS converter was used as a charge amplifier was explained, but the present invention is not limited thereto, and a higher performance solid-state imaging device can also be achieved using a voltage follower, or a differential amplifier that uses an operational amplifier.

In the above embodiment, an explanation was provided using mainly the pixel in the upper left of Fig. 1 as an example, but, of course, the other pixels operate the same way. Further, transfer gates 10-16, horizontal selection switches 26-32, and various other types of switches are controlled by peripheral control circuits, such as a CMOS shift register, CMOS decoder, and the like, which are disposed on a solid-state imaging device chip.

Further, in the above embodiment, the waveband of the light incident on a light-sensitive portion is not clarified, but the present invention can be applied to both the visible light region, and the infrared light region by using a light-sensitive portion having a prescribed waveband.

A solid-state imaging device according to a second embodiment is capable of removing fixed pattern noise and kTC noise (thermal noise), and, in addition, enables the number of elements of a cell, which is the pixel, to be made smaller. Fig. 9 is a diagram showing a circuit of 2 x 2 pixels of a solid-state imaging device in the second

embodiment. A cell CELL in this example has a photodiode 2 for storing a charge corresponding to a quantity of light received, a reset gate 11, which is disposed between reset voltage VRS and photodiode 2, and a transfer gate 10, which is disposed between photodiode 2 and a vertical selection line CLM. Therefore, it is a simple constitution of 2 transistors and 1 photodiode.

And, there is provided a reset control signal line 60 for supplying a reset signal Rn in the horizontal direction, and a transfer gate control signal line 62 for supplying a gate signal TGn, and there are provided vertical selection lines CLMm, CLMm+1, which are connected to the transfer gate 10 of the respective cells in the vertical direction. Similar to the first embodiment, the vertical selection lines are connected to charge amplifiers 41, 43. The charge amplifiers 41, 43 are constituted the same as in the first embodiment, and convert a charge output from a cell CELL to a voltage. Further, charge amplifiers 41, 43 are connected to the respective sample holding and correlated double sampling CDS circuits shown in Fig. 3, and a differential voltage between a reset level and a detection level is generated as a detection signal.

Fig. 10 is a diagram showing the cross-sectional structure, and energy level changes of a cell. Fig. 10A shows the cross-sectional structure of a cell CELL. Inside a P-type substrate 200, which is biased to the

ground, there is formed an N-type well region 100 biased to a power source Vdd, and inside this N-type well region 100, there is formed a P-type well region 111 biased to ground Vss. Therefore, N-type well region 100 is reverse biased, and electrically isolated relative to substrate 200.

Furthermore, P-type well region 111 is formed such that opposite sides are of high concentration, and are deep, and the central portion is of low concentration, and is shallow. In the deep region of the left side, there are formed an n+ region 112, which is connected to reset voltage VRS, and a reset gate electrode Rn, and in the deep region of the right side, there are formed an n+ region 114, which is connected to vertical selection line CLMm, and a transfer gate electrode TGn. And then, in the shallow P-type well region 111A in the central portion, a low-concentration n region 113 is formed. This low-concentration n region 113, and shallow P-type well region 111A form a photodiode PN junction.

On the right side of the cross-sectional view of Fig. 10A, as indicated by the energy level in the depth direction of directly below shallow P-type well region 111A in the center, only a low barrier intervenes between low-concentration n region 113 and N-type well region 100 in accordance with shallow P-type region 111A. Because P-type well region 111A directly below photodiode cathode region 113 is of a low concentration, and thin, and because

N-type well region 100 is biased by power source Vdd, and P-type well region 111 is biased by ground Vss, P-type well region 111A is depleted, and constitutes a low energy level compared to P-type well region 111, which is adjacent to cathode region 113 in the horizontal direction.

Fig. 10B, 10C, 10D, respectively, show energy levels at reset timing t10 and t11, at photoelectrically-converted charge integral timing t12, and at stored charge readout timing t13. Further, Fig. 11 is a timing chart indicating the driving of a cell. A cell readout operation will be explained by referring to these figures.

At reset timing t10, a reset pulse Rn is supplied, reset gate 11 transitions ON, and low-concentration n region 113, which is the cathode region constituting the photodiode, is connected to reset voltage VRS. In accordance therewith, the low-concentration n region 113 of photodiode 2 is completely depleted. In this completely depleted state, the energy level of low-concentration n region 113 constitutes a fixed level determined by the quantity of doped impurities and depth, and thermal noise is not contained in the energy level thereof. When reset pulse Rn disappears, as in Fig. 10C, the barrier of reset gate 11 increases, and the storing of a photoelectrically-converted charge in depleted low-concentration n region 113 begins.

Conversely, separate from reset pulse Rn, at timing t11 immediately prior to readout timing t13, a line reset

pulse LRST is applied to line reset switches 50, 52 of charge amplifiers 41, 43, the input-output terminals of inverters 42, 44 are short-circuited, and vertical selection line CLM is reset to VDD/2. That is, n region 114, which is the drain region of transfer gate 10, is reset to power source intermediate level VDD/2 as reset level VR. Thermal noise is contained in this reset level VR (VDD/2).

By applying line reset signal LRST, the output OUTm of charge amplifier 41 constitutes reset level VR. At that time, a sampling-holding pulse SH is applied, the reset level VR is sampled and held, and, in addition, correlated double sampling capacitor 86 is charged to a level corresponding to the reset level VR.

A photoelectrically-converted charges (since it is n type, an electron) are stored in photodiode low-concentration n region 113 from reset pulse Rn of reset timing t10. In a case in which an excess of light is incident on a pixel at that time, the charges crosse over low barrier 111A in the depth direction of the substrate, the charge flow into N-type well region 100, and the blooming phenomenon, by which charges spill over into an adjacent pixel, is checked. When the above-mentioned integral timing t12 is over, a gate control pulse TGn is applied, and the barrier of transfer gate 10 is lowered, as shown in Fig. 10D. In accordance therewith, the charge stored in low-concentration n region 113 flows into n

region 114. Pursuant thereto, the level of vertical selection line CLMm changes to a rising direction (direction in which potential drops), the level of vertical selection line CLMm is constantly maintained at reset level VDD/2 by an image charging operation of charge amplifier 41, and the potential of output OUTm rises to detection level VS. This detection level is sampled and held, and a differential voltage VS-VR is generated at node N2 of correlated double sampling capacitor 86.

In this case, because initial thermal noise is also superimposed on detection level VS, thermal noise is removed from the differential voltage VS-VR. Naturally, fixed pattern noise is not contained in differential voltage VS-VR.

As a characteristic of the second embodiment, there provides a reset gate 11 for removing a charge stored in the well of photodiode 2. Moreover, when this reset gate 11 is ON, the electron well of photodiode 2 is completely depleted, and is reset to an absolute level determined by the doping concentration and depth of low-concentration n region 113. Therefore, thermal noise is not contained therein. And by controlling the timing at which reset pulse Rn is applied, it is possible to achieve either an electron shutter function, or a exposure control function.

Fig. 12 is a diagram showing a variation of the second embodiment. As shown in the cross-sectional view of Fig. 12A, the P-type well region 111 of the central portion

is formed deeply, and a low-concentration n region 113, which forms a photodiode 2, is formed therein. Therefore, there is no blooming suppressing function that uses a shallow P-type well region 111A as shown in Fig. 10A. In place thereof, in the example of Fig. 12, by applying a low potential reset pulse Rn to reset gate 11 and continuing a quasi-conductive state without setting reset gate 11 completely OFF at integral timing t12, which stores photoelectrically-converted electrons, when an excess of light is received at integral timing t12, electrons leaked to the n region 112 side to which reset voltage VRS is applied. In accordance therewith, the blooming phenomenon, whereby a charge resulting from excess light spills over to an adjacent pixel, is prevented from occurring.

Fig. 13 is a diagram showing simulation results of a case in which a cell circuit of the second embodiment is utilized. As also shown in Fig. 11, output VOUT is reset to nearly VDD/2 (VR) by a reset operation, and thereafter, increases to the detection level VS by setting the transfer gate to ON. Therefore, in the second embodiment, because the output VOUT of a charge amplifier only rises from reset level VR to detection level VS, the upper half of the power source VDD (= 3V) range of CMOS inverters 42, 44 is mainly used. By contrast thereto, in the first embodiment, as shown in Fig. 6, output VOUT drops one time to reset level VR from VDD/2, and rises to detection level VS. That is,

the dynamic range relative to differential voltage (VS-VR) is broader in the first embodiment.

Therefore, in the second embodiment, the dimension ratio of the P-channel transistor and the N-channel transistor of a CMOS inverter is changed, so that the operating point is set lower than VDD/2. In accordance therewith, it is possible to make reset level VR lower than VDD/2, enabling the realization of a broad dynamic range like that in the first embodiment.

In the above second embodiment as well, a cell photodiode can be replaced by a photogate as shown in Fig. 4E. In this case, too, the electron well directly below the photogate gate oxide layer is depleted by making the reset gate conductive, and reset to an absolute level, which is determined by concentration conditions and so forth.

As described hereinabove, according to the present invention, it is possible to achieve a solid-state imaging device, which has a simple pixel constitution, and a wide numerical aperture, and which reduces fixed pattern noise (FPN) and thermal noise (kTC noise).

What Is Claimed Is:

1. A solid-state imaging device comprising:

a plurality of pixels, including a light-sensitive portion for photoelectrically converting incident light, a transfer gate for transferring a charge stored in said light-sensitive portion, a resettable detection capacitor for storing said charge transferred from said transfer gate, and a selection switch for outputting a charge of said detection capacitor according to of a selection signal;

a charge amplifier for converting to a voltage said detection capacitor charge, which is outputted from the pixels, and a correlated double sampling circuit for obtaining a voltage difference between a reset level and a detected level converted by the charge amplifier.

2. The solid-state imaging device according to claim 1, wherein said charge amplifier is a capacitive feedback-type impedance conversion circuit.

3. The solid-state imaging device according to claim 1, wherein said charge amplifier converts to a reset voltage a reset level of said detection capacitor by said selection switch transitioning to ON, and said detection capacitor being connected to an input of said charge amplifier, and thereafter, converts to a detection signal voltage said charge, which was transferred to said

detection capacitor from said light-sensitive portion by said transfer gate transitioning to ON.

4. A solid-state imaging device comprising:

a plurality of pixels, including a light-sensitive portion for photoelectrically converting incident light and storing a charge, a reset gate connected to said light-sensitive portion, and depleting said light-sensitive portion by becoming conductive in response to a reset signal, and a transfer gate, connected to said light-sensitive portion, for outputting a charge stored in said light-sensitive portion by becoming conductive in response to a selection signal;

a charge amplifier, connected to said pixel, for converting said outputted charge to a voltage; and

a correlated double sampling circuit for sampling and holding an output voltage of said charge amplifier,

wherein a differential voltage between a reset level which said charge amplifier outputs when being reset, and a detection level, which said charge amplifier outputs in accordance with a charge outputted from said pixel, is outputted from said correlated double sampling circuit.

5. The solid-state imaging device according to claim 4, wherein said light-sensitive portion is formed by a second conductive-type cathode region, which is

formed at a prescribed depth inside a first conductive-type semiconductor region, and

said reset gate is a MOS-type transistor, which is formed by said cathode region, a reset gate electrode formed on said first conductive-type semiconductor region, and a second conductive-type drain region, which is formed inside said first conductive-type semiconductor region, and which has a higher concentration than said cathode region.

6. The solid-state imaging device according to claim 5, wherein said transfer gate is a MOS-type transistor, which is formed by said cathode region, a transfer gate electrode formed on said first conductive-type semiconductor region, and a second conductive-type output region, which is formed inside said first conductive-type semiconductor region, and which is connected to an input of said charge amplifier.

7. The solid-state imaging device according to claim 4, wherein said first conductive-type semiconductor region is formed inside a second conductive-type well region, and is controlled such that a region directly beneath said cathode region of said well region is depleted.

8. The solid-state imaging device according to

claim 5, wherein said first conductive-type semiconductor region is formed inside a second conductive-type well region, and is controlled such that a region directly beneath said cathode region of said well region is depleted.

9. The solid-state imaging device according to claim 4, wherein said reset gate maintains a quasi-conductive state while said light-sensitive portion stores a photoelectrically-converted charge.

ABSTRACT

A solid-state imaging device comprises: a plurality of pixels including a light-sensitive portion (2) for photoelectrically converting incident light, a transfer gate (10) for transferring a charge stored in the light-sensitive portion, a resettable detection capacitor (18) for storing the charge transferred from the transfer gate, and a selection switch (26) for outputting a charge of the detection capacitor according to a selection signal RWn; a charge amplifier (41) for converting the detection capacitor charge, which is outputted from the pixels, to a voltage; and a correlated double sampling circuit (86) for obtaining a voltage difference between a reset level and a detected level converted by the charge amplifier. According to the above device, a thermal noise is eliminated due to the correlated double sampling circuit. Further, a fixed pattern noise is not generated due to the pixel circuit structure.

FIG. 1

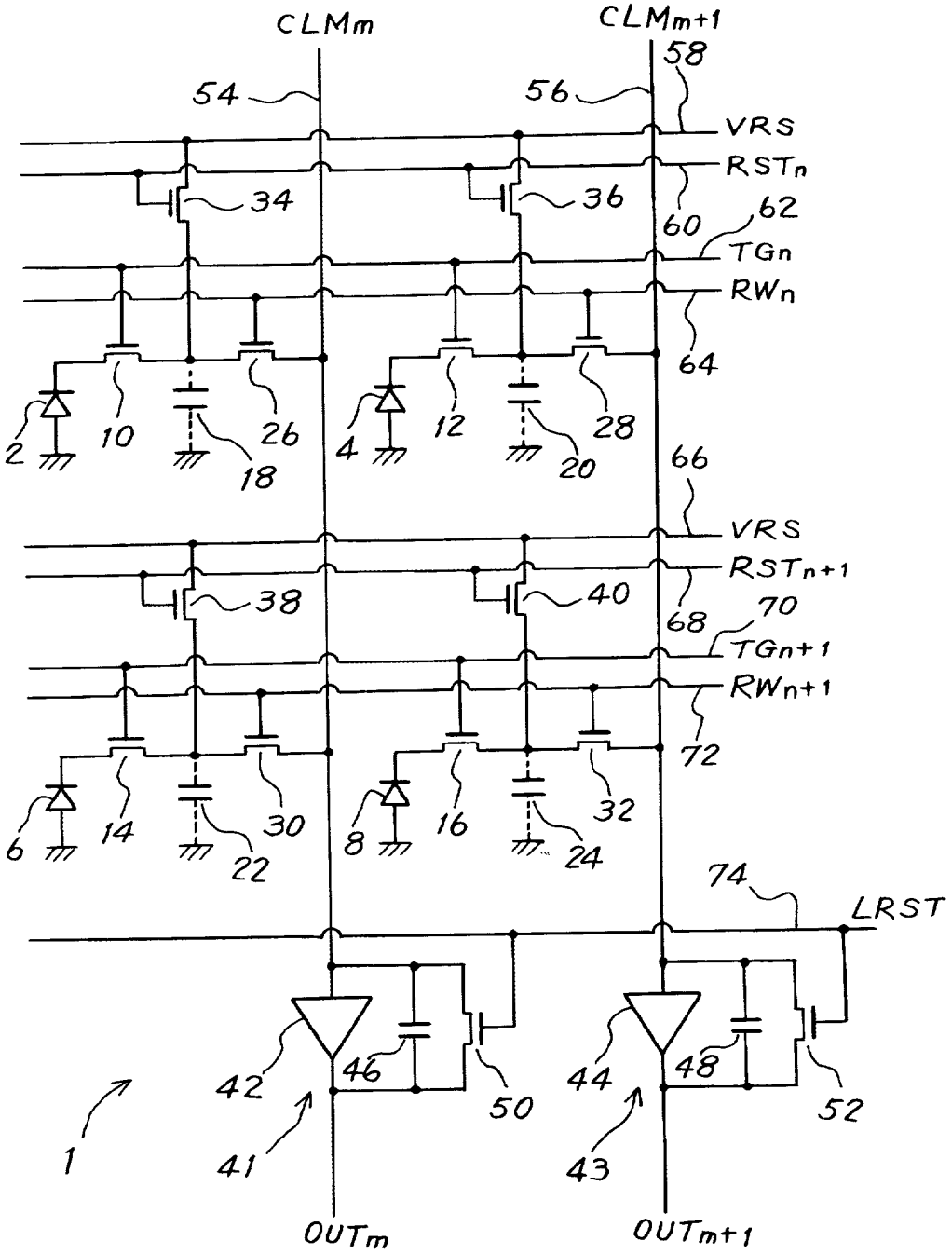

CLMm
CLMm+1
54
56
58
VRS
RSTn
34
36
60
62
TGn
RWn
64
2
10
26
18
4
12
28
20
66
VRS
RSTn+1
38
40
68
70
TGn+1
RWn+1
72
6
14
30
22
8
16
32
24
74
LRST
42
46
50
44
48
52
1
41
43
OUTm
OUTm+1

FIG. 2

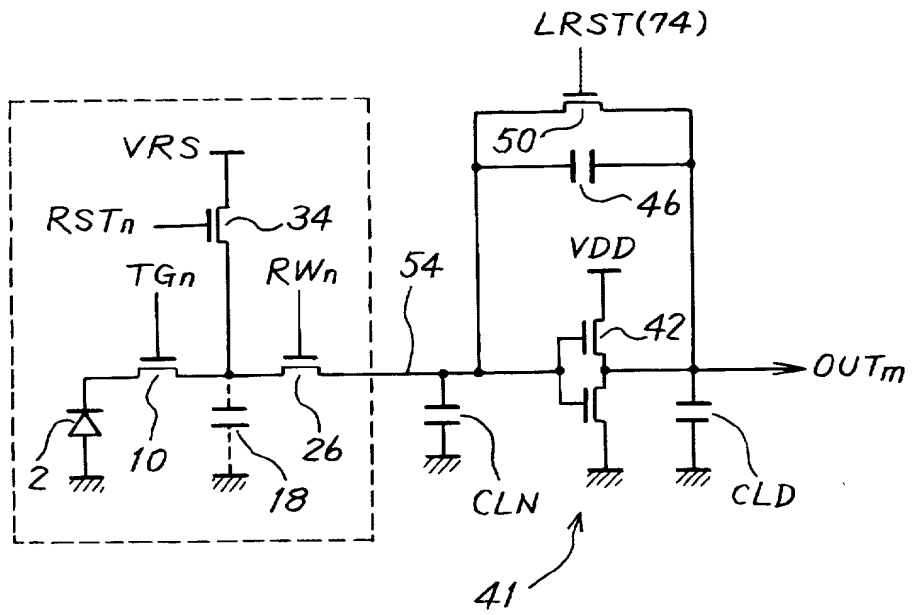

LRST(74)
50
46
VRS
RSTn
34
TGn
RWn
54
VDD
42
OUTm
2
10
26
18
CLN
CLD
41

FIG. 3

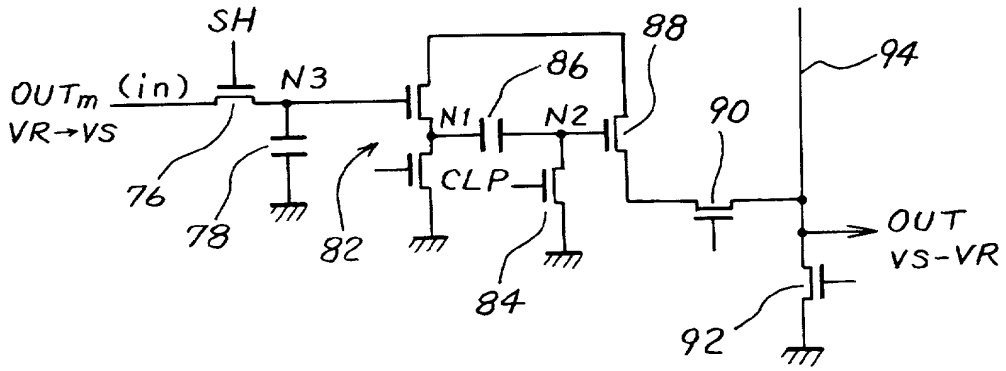

SH
OUTm (in)
VR→VS
N3
86
88
94
N1
N2
90
76
78
82
CLP
84
OUT
VS-VR
92

FIG. 4A

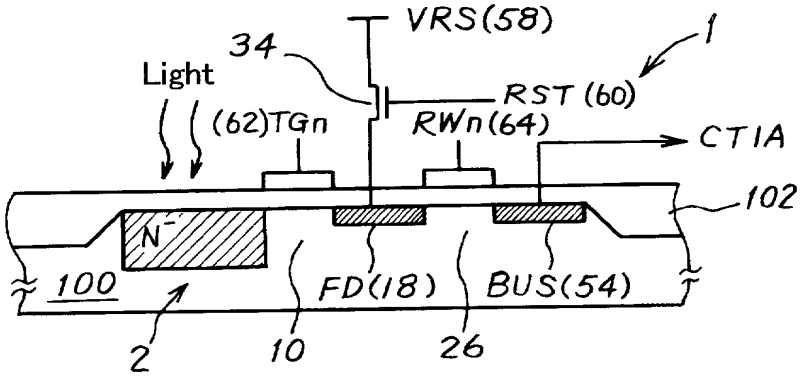


FIG. 4B

Reset Period t1

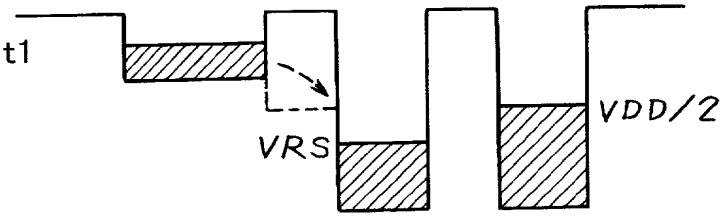


FIG. 4C

Reset Level
Read out Period t2

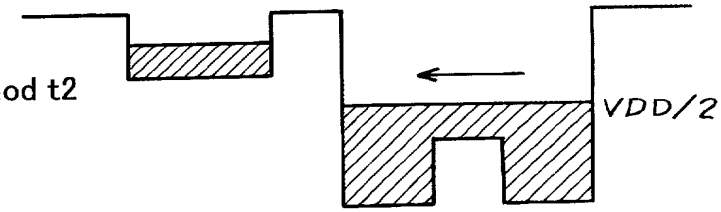


FIG. 4D

Light Integral Value
Read out Period t3

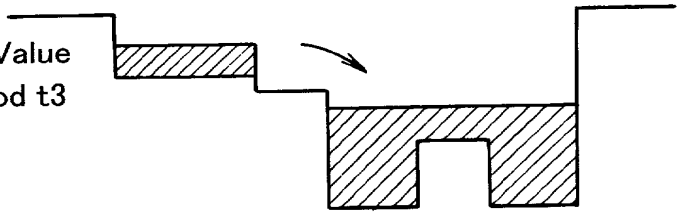


FIG. 4E

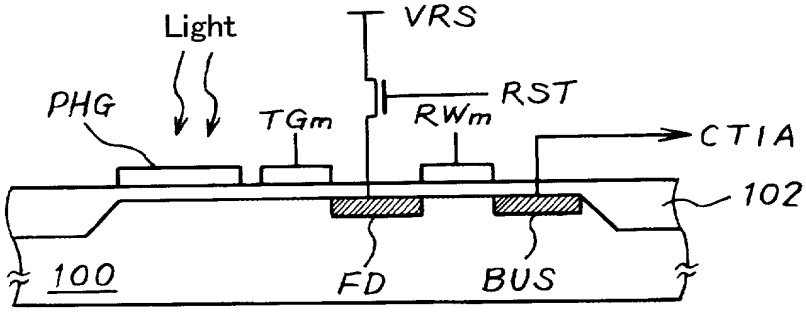


FIG. 5

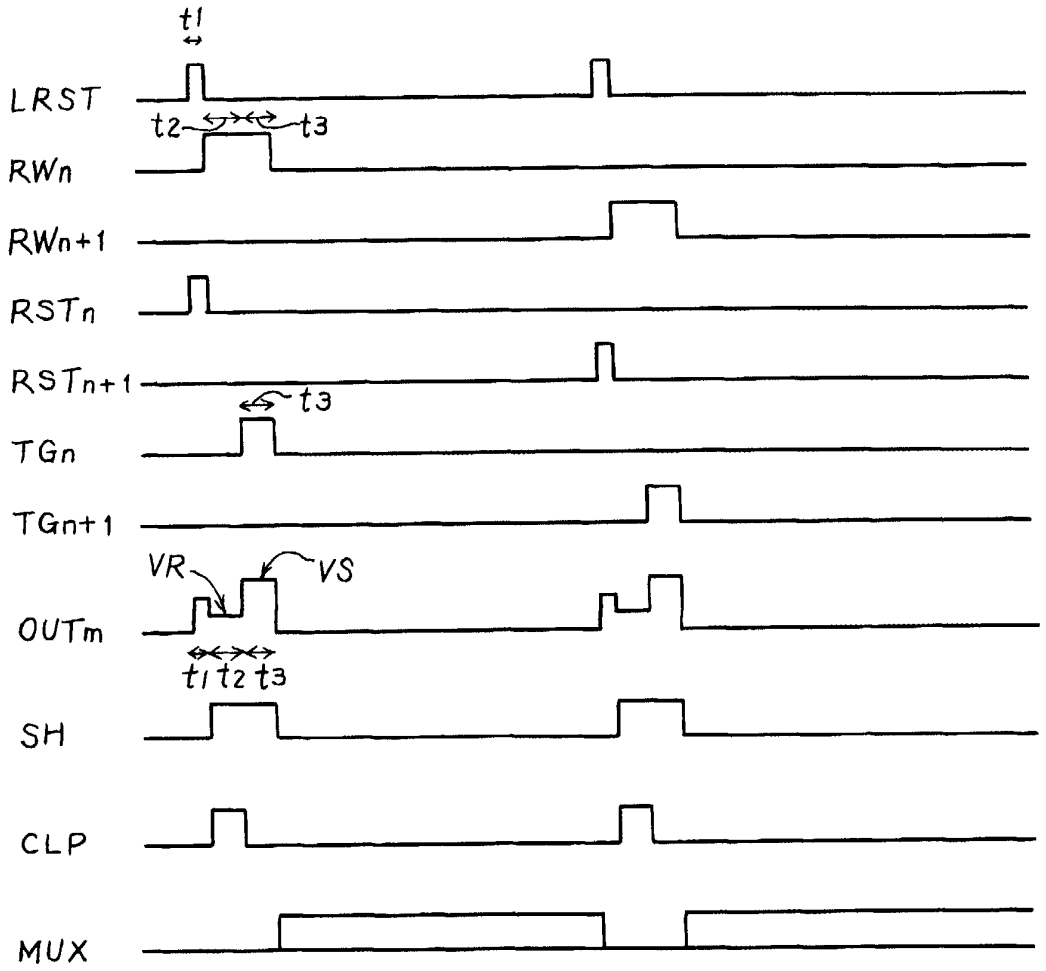

t1
LRST
t2
t3
RWn
RWn+1
RSTn
RSTn+1
t3
TGn
TGn+1
VR
VS
OUTm
t1 t2 t3
SH
CLP
MUX

FIG. 6

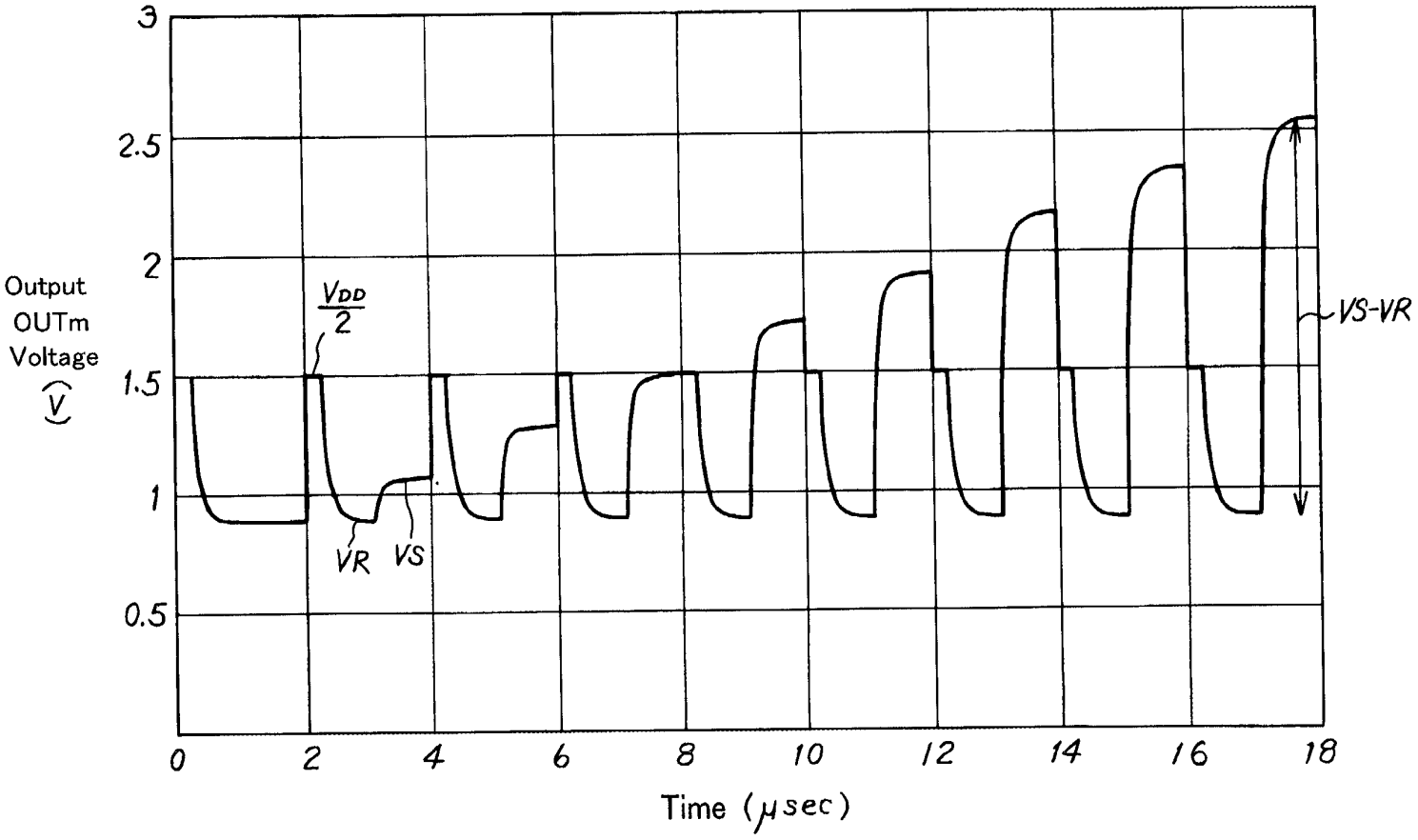

3
2.5
2
1.5
1
0.5
Output
OUTm
Voltage
V
VDD/2
VR
VS
VS-VR
0
2
4
6
8
10
12
14
16
18
Time (μsec)

FIG. 7

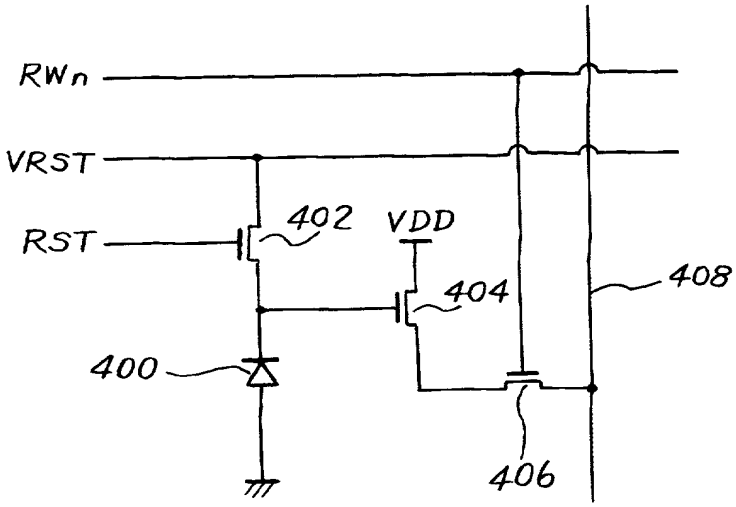

RWn
VRST
RST
402
VDD
404
408
400
406

FIG. 8

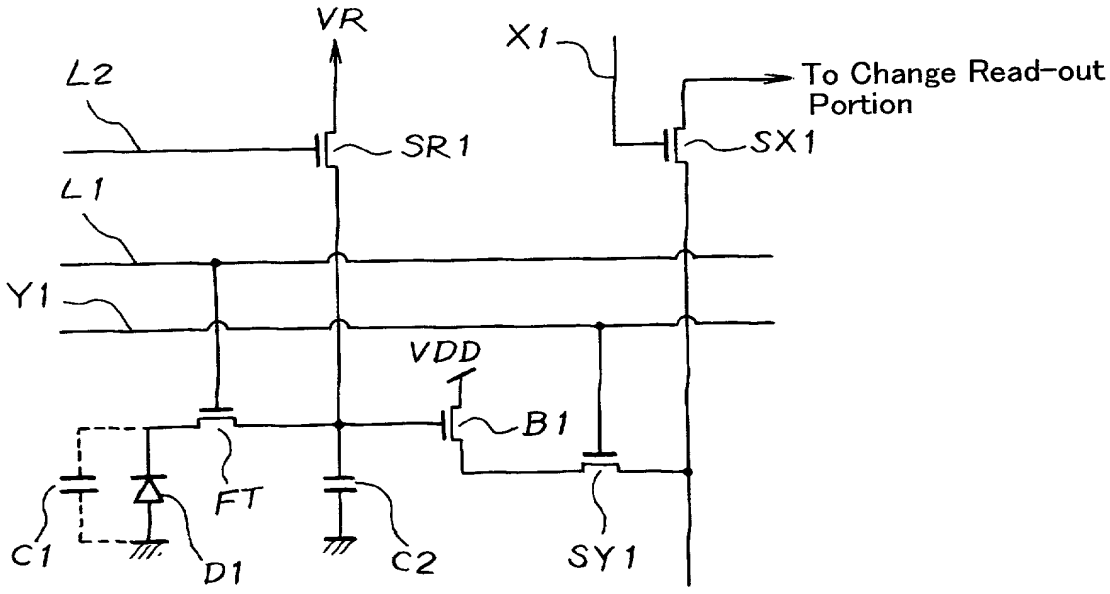

VR
X1
To Change Read-out Portion
L2
SR1
SX1
L1
Y1
VDD
B1
FT
C1
D1
C2
SY1

FIG. 9

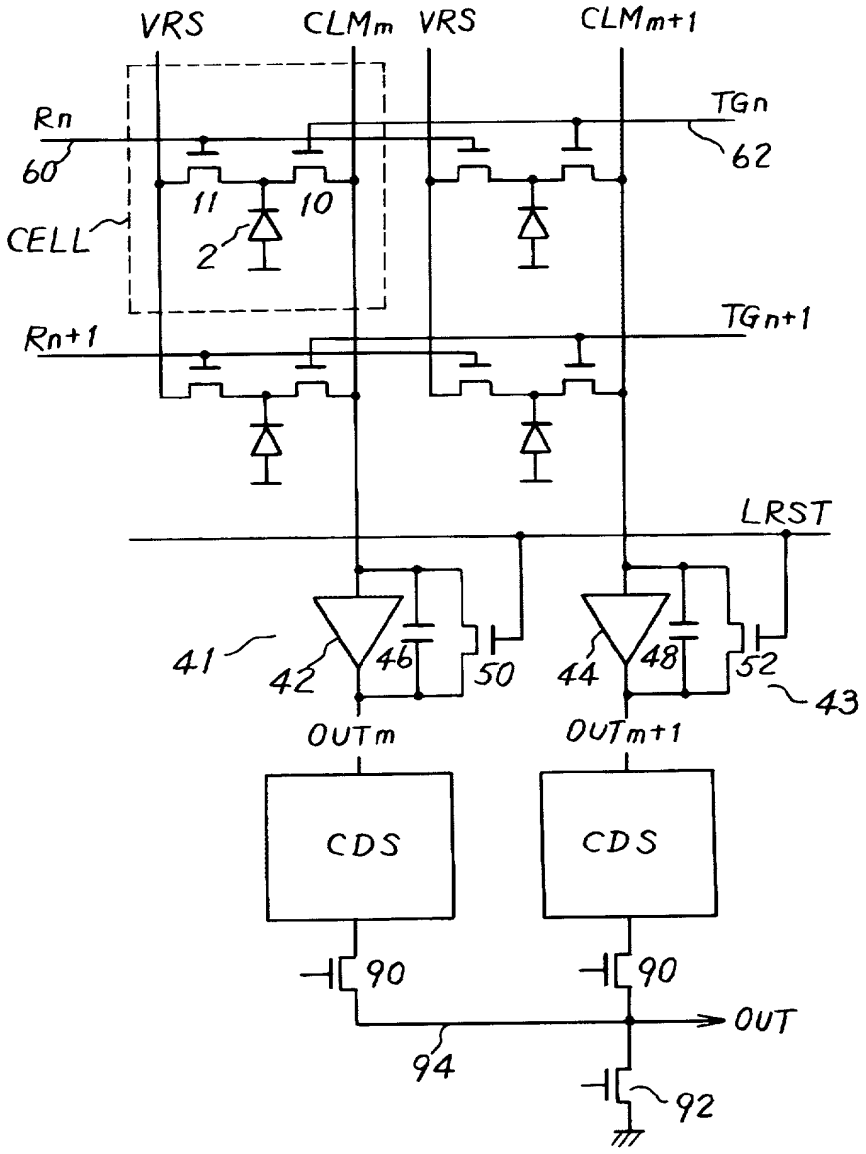

VRS
CLMm
VRS
CLMm+1
Rn
60
TGn
62
11
10
CELL
2
Rn+1
TGn+1
LRST
41
42
46
50
44
48
52
43
OUTm
OUTm+1
CDS
CDS
90
90
OUT
94
92

FIG. 10A

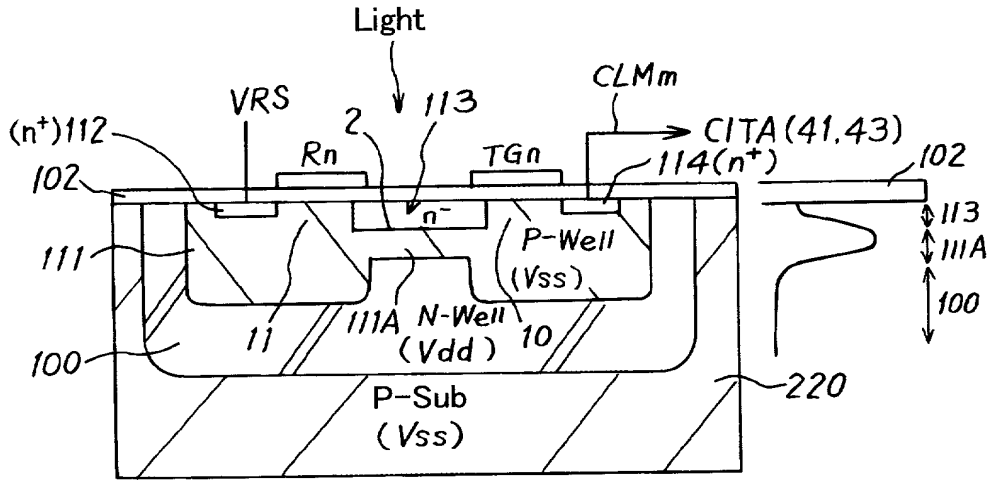


FIG. 10B

t10,t11

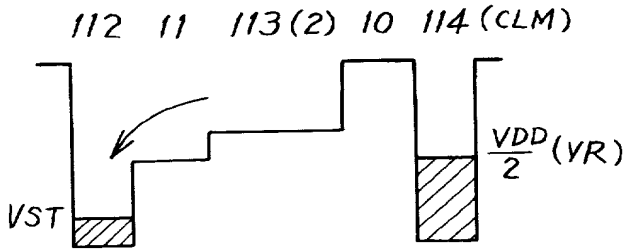


FIG. 10C

t12

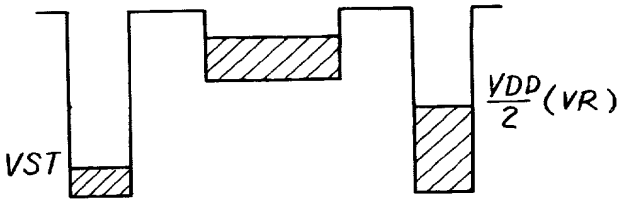


FIG. 10D

t13

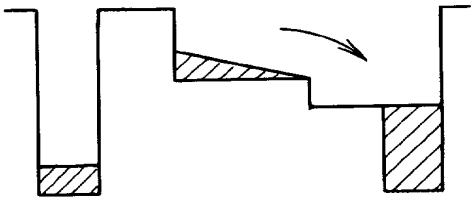


FIG. 11

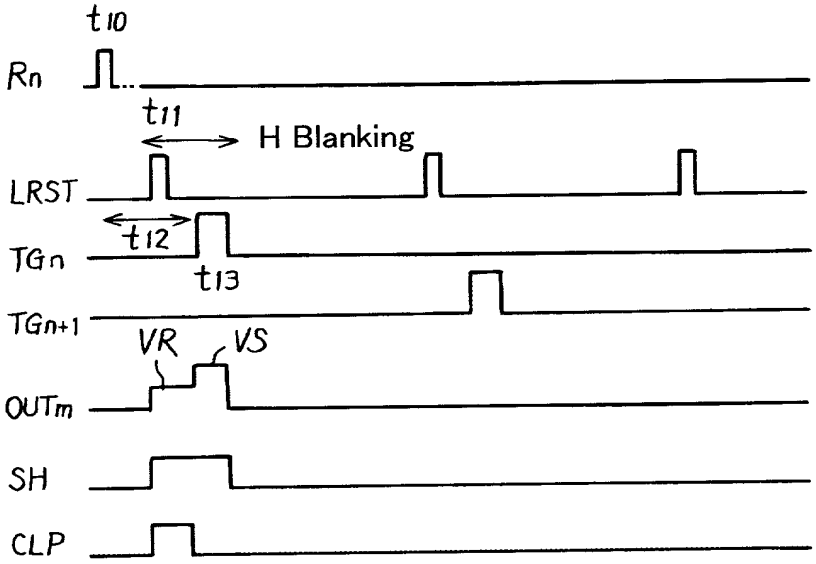


FIG. 12A

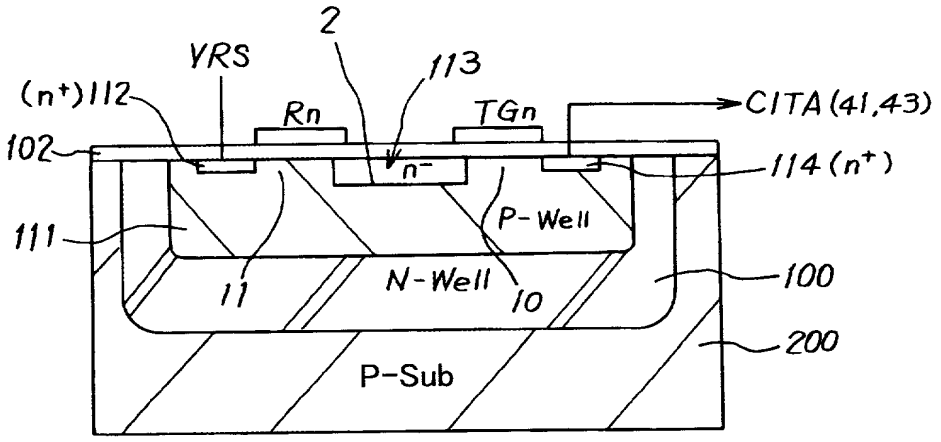


FIG. 12B
t_{10}, t_{11}

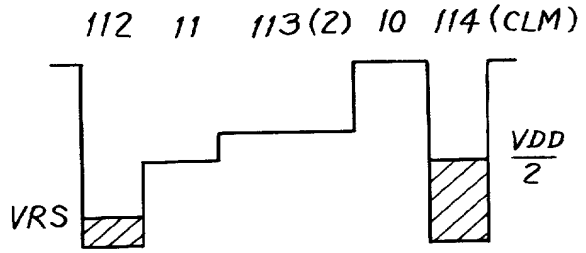


FIG. 12C
t_{12}

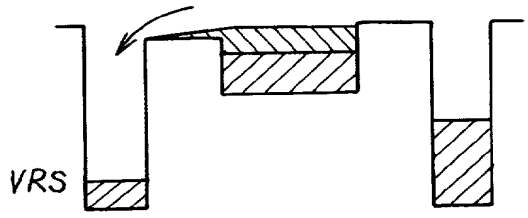


FIG. 12D
t_{13}

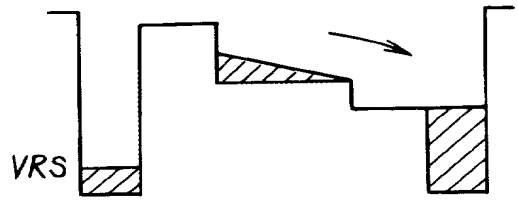
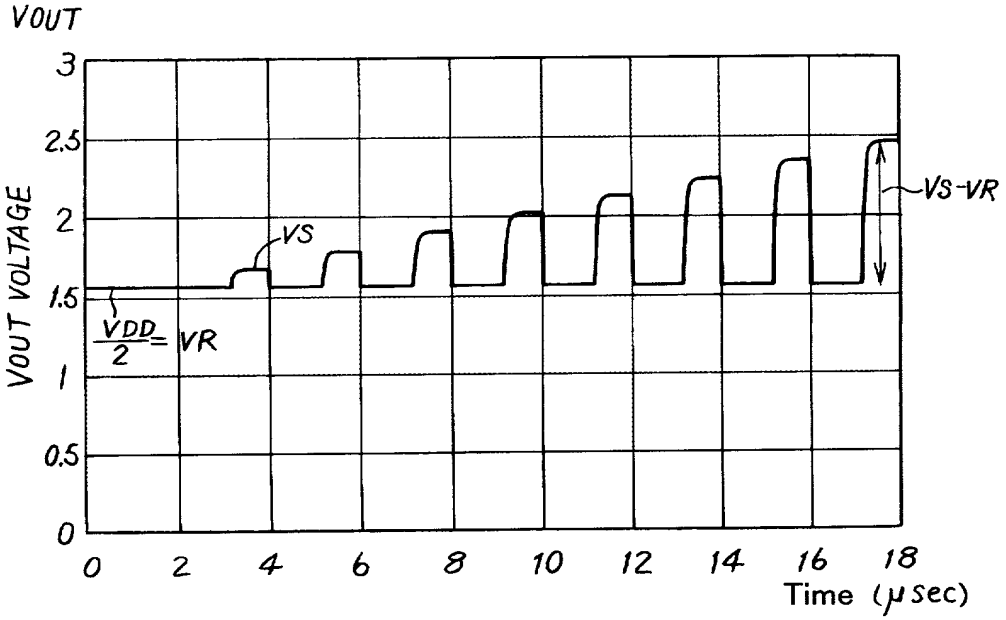


FIG. 13


VOUT
3
2.5
2
1.5
1
0.5
0
VOUT VOLTAGE
VS
VS-VR
VDD/2 = VR
0
2
4
6
8
10
12
14
16
18
Time (μsec)

Declaration and Power of Attorney for U.S. Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SOLID-STATE IMAGING DEVICE

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ _月_日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____ に訂正されました。

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条(a)-(d)項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約３６５(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
11-182589 (Number) (番号)	Japan (Country) (国名)	28/06/1999 (Day/Month/Year Filed) (出願年月日)	☐
2000-158023 (Number) (番号)	Japan (Country) (国名)	29/05/2000 (Day/Month/Year Filed) (出願年月日)	☐

私は、第３５編米国法典１１９条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(c)に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに下記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

See list of attorneys and/or agents on page 5.

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第二共同発明者 日付	Second inventor's signature Date
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国籍	Citizenship
私書箱	Post Office Address

（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)

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国籍		Citizenship	
私書箱		Post Office Address	
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第四発明者の署名	日付	Fourth inventor's signature	Date
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私書箱		Post Office Address	
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第五発明者の署名	日付	Fifth inventor's signature	Date
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国籍		Citizenship	
私書箱		Post Office Address	
第六共同発明者		Full name of sixth joint inventor, if any	
第六発明者の署名	日付	Sixth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	

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